A 1.8-V Pseudo-Differential Second-Order Closed-Loop VCO ΔΣ ADC with Brick-Wall Active Clamp and Isolated Digital Feedback in 130-nm CMOS

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Open-Source Silicon Tapeout: Tiny Tapeout SKY26e (`sky130A` *130-nm CMOS,* 1×2 *Analog Tile* `tt_um_arcadia1_vco_adc`*,* $161.0 \times 225.76\,\mu m^2$*)*

***Abstract*—This report presents the design, verification, and physical sign-off of `tt_um_arcadia1_vco_adc`, a 1.8-V pseudo-differential second-order continuous-time closed-loop VCO ΔΣ ADC in `sky130A` ($161.0 \times 225.76\,\mu m^2$ Tiny Tapeout 1×2 tile, $f_s = 10$ MHz, BW = 50 kHz, OSR = 100, ±0.60 V diff. full scale around 0.90 V). Each half cascades a common-centroid 5T OTA-C integrator with a 7-stage current-starved ring VCO, two-rank XOR phase differentiator, and intrinsically barrel-shifted 7-element NRZ RDAC. Three upgrades over S13 eliminate key silicon risks: (1) upsizing the OTA (48/3 μm NMOS, 16/2 μm PMOS, 23 μA tail) lowers BSIM4 $1/f$+thermal noise by +10.2 dB (74.6 → 22.9 μV_{rms}, 79.3 dB ceiling, 85.3 dB FS DR, Tian PM = 72.2°); (2) a zero-static-power 5-FET Miller-compensated active clamp (`CLAMP_A5`, 14.3–48.9 nA @ 1.15 V, 0.00 dB noise/HD3 penalty) hard-limits $f_{VCO} \le 6.66$ MHz below 7.5 MHz aliasing latch-up; and (3) dedicated `buf_4` pin buffers cut BSIM4 XOR glitch charge theft 19×–90× and rise/fall asymmetry 20×–215× over C_{load} = 1–5 pF. True in-band 14.65 kHz (HD3 = 43.95 kHz in-band) sign-off achieves 71.8 dB TT schematic SNDR (68.5–73.4 dB across 17 1.80/1.98 V PVT+R/C corners; 71.1 dB median across 16 `tt_mm` MC seeds) and 69.0–70.6 dB SNDR (77.7–81.9 dB SNR, HD3 = −70.4 to −72.5 dBc) across all 6 full-transistor flat-PEX corners (173.4 μW core / 312 μW PEX w/ 16×1 pF), with 0 DRC, unique LVS (54/54 pins), 16/16 TT precheck, and 4/4 flat-PEX latch-up stress passes.**

***Index Terms*—Continuous-time ΔΣ ADC, VCO-based quantizer, second-order noise shaping, active Miller clamp, digital output isolation, `sky130A`, Tiny Tapeout.**

I. Introduction

Voltage-controlled oscillator (VCO)-based analog-to-digital converters replace power-hungry comparators and precision multibit DACs with compact, time-domain phase quantizers that naturally scale with CMOS technology [1, 2]. Operated open-loop, however, a ring oscillator exhibits severe static $f_{VCO}(V_{ctrl})$ nonlinearity that limits distortion to 40–50 dB. Embedding the ring VCO inside a continuous-time negative-feedback loop preceded by an active OTA-C integrator solves both problems: loop gain suppresses VCO nonlinearity in-band, the cascade of integrator and VCO phase integration yields true second-order (40 dB/dec) noise shaping, and sampling all $M = 7$ ring phases provides a 7-level quantizer whose phase rotation implements first-order intrinsic dynamic element matching (DEM) across the resistor DAC [1, 3].

This work implements a pseudo-differential second-order closed-loop VCO ΔΣ ADC (`tt_um_arcadia1_vco_adc`) within a Tiny Tapeout SKY26e 1×2 analog tile ($161.0 \times 225.76\,\mu m^2$, single 1.8 V supply `VDPWR`, analog inputs `ua[0:1]`, digital outputs `uo_out[7:0]` and `uio_out[7:0]`). Deep verification of the initial baseline layout (`Base_S13`) revealed three latent silicon risks masked by nominal noiseless transient simulations:

1. **OTA $1/f$ Noise Ceiling:** A compact 8/1 μm input pair produced 74.6 μV_{rms} BSIM4 noise (100 Hz–50 kHz), capping real silicon SNR at 69.1 dB despite 75–81 dB noiseless FFTs.
2. **Phase-Aliasing Latch-Up ($f_{VCO} > 0.75 f_s$):** During unreset startup or rail overload at fast-NMOS/low-R high-V_{DD} corners (`fs_ll`/1.98 V, `ss_ll`/85°C/1.98 V), v_{ctrl} saturated toward V_{DD}, driving f_{VCO} to 7.85–9.33 MHz. Above $0.75 f_s = 7.5$ MHz, XOR differentiation aliases backward and inverts feedback polarity, permanently latching the ring near 8.5 MHz.
3. **External Load Coupling into Feedback DAC:** Driving external 1–5 pF pad/mux capacitance directly from first-rank `dfxtp_4` skewed `Q1` vs. `Q2` at `xor2_1`, causing full-rail glitches that stole up to 14.8 ns of DAC charge and injected 6.0 ns rise/fall asymmetry.

The finalized `V2_A5` revision resolves all three vulnerabilities with zero clamping static power and complete physical sign-off. Table I summarizes the specifications and verified gains over `Base_S13`.

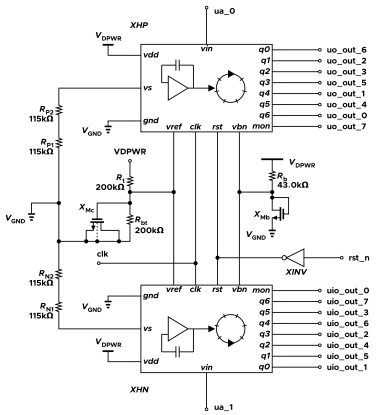
II. Circuit Architecture and Design Choices

Fig. 1 depicts the full hierarchy of `tt_um_arcadia1_vco_adc`. Two mirror-image halves (`XHP`, `XHN`) process complementary inputs `VINP` (`ua[0]`) and `VINN` (`ua[1]`) around $V_{ref} = V_{DD}/2 = 0.90$ V while sharing a resistive V_{ref} divider ($R_t = R_{bt} = 200.4\,k\Omega$ decoupled by a $10 \times 10\,\mu m^2$ NMOS cap X_{Mc}), an OTA tail bias mirror ($R_b = 42.3\,k\Omega$ into 8/2 μm diode X_{Mb}), a common-centroid VCO degeneration resistor array ($D\,N_1\,P_1\,P_2\,N_2\,D$, $R_{vco} = 229.7\,k\Omega$/half), an active-low reset inverter, and eight dedicated `conb_1` tie-high cells for `uio_oe[7:0]`.

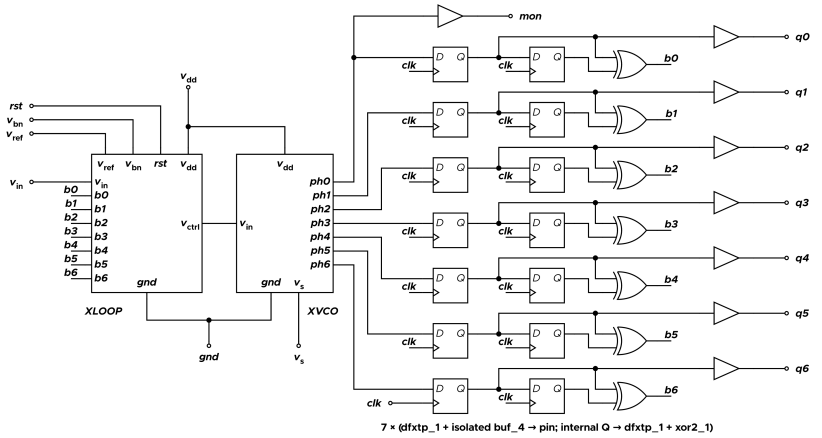
A. Pseudo-Differential Loop and Intrinsic DEM

In each half (Fig. 1c), the input drives $R_{in} = 49.7\,k\Omega$ (`res_xhigh_po_0p35`, $L = 8.6\,\mu m$) into virtual ground v_g of an inverting OTA-C integrator using two $24 \times 25\,\mu m^2$ metal-3 MIM capacitors ($C_{int} = 2.43$ pF) and a 0.42/0.15 μm NMOS reset switch X_{Mr}. Output v_{ctrl} controls a 7-stage current-starved ring VCO via source-degenerated V-to-I NMOS XM_1 (4/1 μm) over $R_{vco} = 229.7\,k\Omega$ and a 1:1 PMOS/NMOS mirror (1/1 μm PMOS, 0.5/1 μm NMOS, 1.4/2.86 μm MOS stage load caps).

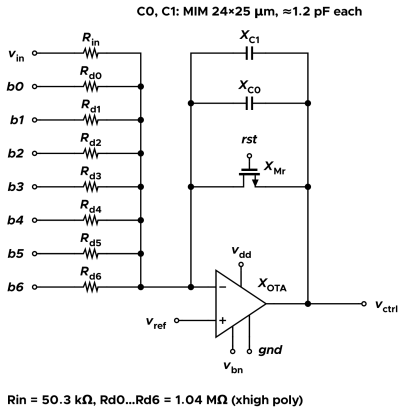
On each rising edge of $f_s = 10$ MHz, seven first-rank `dfxtp_1` flip-flops sample ring phases $ph_0 \ldots ph_6$, while second-rank `dfxtp_1` and `xor2_1` gates form transition bits $b_i[n] = Q_{1,i}[n] \oplus Q_{1,i}[n-1]$ on-chip. Each rail-to-rail NRZ bit drives one element ($R_d = 1.04\,M\Omega$, $L = 181.8\,\mu m$) of a 7-element resistor DAC into v_g. Because R_{in} and $R_{d,0\ldots6}$ share the iden-



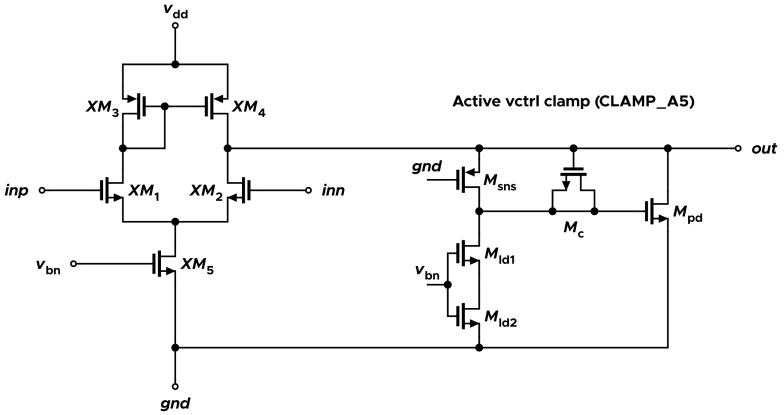
(a) Top-level pseudo-differential tile.



(b) One half-channel: loop, 7-stage VCO, and isolated digital backend (`dfxtp_1` + `buf_4`).



(c) OTA-C integrator & 7-element RDAC.



(d) 5T OTA with 5-FET Miller-compensated brick-wall active clamp (`CLAMP_A5`).

Fig. 1. Complete schematics of `tt_um_arcadia1_vco_adc` (`V2_A5`): (a) mirrored P/N halves sharing V_{ref}, OTA bias, and common-centroid VCO bias resistors; (b) half-channel loop with `buf_4`-isolated external outputs; (c) continuous-time integrator ($R_{\text{in}} = 49.7\,\text{k}\Omega$, $7 \times R_d = 1.04\,\text{M}\Omega$, $C_{\text{int}} = 2.43$ pF); and (d) low-noise common-centroid 5T OTA with the 5-FET Miller-compensated brick-wall active clamp `CLAMP_A5`.

tical `res_xhigh_po_0p35` material and strip pitch (42 strips plus dummies), absolute sheet-resistance spread cancels in full-scale gain, and natural ring phase rotation provides first-order barrel-shifter DEM without digital DEM overhead. Off-chip DSP computes $y_P[n] = \sum_i (Q_{P,i}[n] \oplus Q_{P,i}[n-1])$, $y_N[n]$ likewise, and $y[n] = y_N[n] - y_P[n]$, cancelling even-order distortion and common-mode V_{ref}/supply drift. At mid-scale, each loop holds an average code of 3.5, locking $f_{\text{VCO}} = f_s/4 = 2.50$ MHz across PVT.

B. Low-Noise Common-Centroid 5T OTA

Front-end OTA input-referred noise adds directly to V_{in} multiplied by noise gain $(1 + R_{\text{in}}/R_{d,\text{eq}}) = 1.335$. In `Base_S13`, the $8/1\,\mu$m NMOS pair and $8/1\,\mu$m PMOS load suffered 98.0% $1/f$-dominated noise ($74.6\,\mu\text{V}_{\text{rms}}$). In `V2_A5`, $XM_{1,2}$ are enlarged 18× in gate area to $48/3\,\mu$m ($4 \times 12/3\,\mu$m common-centroid `A A B B B B A A`), $XM_{3,4}$ are enlarged 4× to $16/2\,\mu$m ($4 \times 4/2\,\mu$m), and XM_5/XM_b are doubled to $8/2\,\mu$m ($I_{\text{tail}} = 23.0\,\mu$A). This cuts $1/f$ noise variance by 14.4× (+10.2 dB SNR ceiling to 79.3 dB), boosts DC gain 43.0 → 47.8 dB and GBW 7.9 → 14.7 MHz, and reduces 1-LSB virtual-ground kickback from 51.5 to 32.2 mV.

C. Phase-Aliasing Latch-Up and Brick-Wall Clamp (`CLAMP_A5`)

For an $M = 7$-stage ring sampled at $f_s = 10$ MHz, monotonic XOR phase differentiation spans $f_{\text{VCO}} \in (0, f_s/2) = (0, 5\,\text{MHz})$. Between 5.0 and 7.5 MHz, aliased XOR counts remain > 3.5

TABLE I
SPECIFICATION SUMMARY AND VERIFICATION PROGRESSION (`Base_S13` VS. FINAL `V2_A5`)

Metric / Parameter	Target / Constraint	Baseline (`Base_S13`)	Final Design (`V2_A5`)
Process / Tile Footprint	`sky130A`, 1 × 2 TT tile	$161.0 \times 225.76\,\mu\text{m}^2$	$161.0 \times 225.76\,\mu\text{m}^2$ (699 × `decap_12`)
Supply / Clock / BW / OSR	1.8 V ± 10%, 10 MHz, 50 kHz, 100	1.8 V, 10 MHz, 50 kHz, 100	1.8 V ± 10%, 10 MHz, 50 kHz, 100
Full-Scale Input (Diff. / Side)	±0.60 V diff (±0.30 V/side @ 0.9 V)	±0.60 V diff	±0.60 V diff ($R_{\text{in}} = 49.7\,\text{k}\Omega$)
OTA DC Gain A_0 / GBW (TT)	> 45 dB / > 10 MHz	43.0 dB / 7.9 MHz	**47.8** dB / **14.7** MHz
Tian Loop PM / GM (PVT)	> 60° / > 6 dB	Unclamped (v_g step 51.5 mV)	**72.2**° [67.7°–79.8°] / **6.5** dB [6.5–7.2]
BSIM4 Diff. Noise (0.1–50 kHz)	< 30 μV_{rms} (> 77 dB @ 0.15 V/s)	74.6 μV_{rms} (69.1 dB; 75.1 dB FS)	**22.9** μV_{rms} (**79.3** dB; **85.3** dB FS, +**10.2** dB)
Clamp Noise / HD3 Penalty	0.0 dB	N/A (no clamp)	**0.00** dB (14.3–48.9 nA @ 1.15 V)
Anti-Latchup Stress (Sch. / PEX)	f_{max} < 7.5 MHz, 100% recovery	**FAIL** (latched 7.85–8.49 MHz)	**PASS** (10/10 sch., 4/4 PEX; $f_{\text{cl}} \le 6.66$ MHz)
Dig. Isolation Glitch / Asym.	Invariant over C_{load} = 1–5 pF	1.92–14.82 ns / 0.58–6.01 ns	**0.10–0.16** ns (19–90×) / **0.029** ns (20–215×)
In-Band 14.65 kHz SNDR (Sch./PEX)	> 69 dB (HD3 = 43.95 kHz in-band)	PEX `sf` HD3 −59.0 dBc; latch risk	**71.8** dB sch. / **69.0–70.6** dB flat-PEX (6/6)
21-Corner PVT+R/C (1.8/1.98 V)	> 68 dB nominal/high-V_{DD}	Untested across R/C+V_{DD}	**68.5–73.4** dB (med. 71.2 dB, 21/21 lock)
16-Seed `tt_mm` Mismatch MC	Median > 70 dB, tight offset	Untested	**68.1–71.7** dB (med. **71.1** dB, σ = 1.17 dB)
Core Power / PEX (16 × 1 pF)	< 350 μW @ 1.8 V	~ 260 μW (w/ 1 pF loads)	**173.4** μW core (**312.3** μW flat-PEX TT)
Physical Sign-Off (DRC/LVS/TT)	0 DRC, Clean LVS, 16/16 Precheck	0 DRC, `uio_oe` LVS warn	**0 DRC**, **Unique LVS** (54/54 pins), **16/16 TT**

(negative feedback), but for $f_{\mathrm{VCO}} > 0.75 f_s = 7.5$ MHz the mean feedback code drops *below* 3.5, inverting loop polarity into positive-feedback latch-up near 8.5 MHz during unreset startup or rail overload at fast-NMOS/low-R corners ($f_{\mathrm{unclmp}} = 9.0$–$9.3$ MHz).

A 1-FET PMOS diode clamp ($8/0.5\,\mu$m) prevents runaway, yet its soft subthreshold knee leaks 1.1–4.5 μA at $v_{\mathrm{ctrl}} = 1.15$ V, degrading `ff_hh`/−20°C in-band HD3 to −46 dBc. Instead, `V2_A5` integrates the 5-FET all-standard-V_t Miller-compensated active clamp `CLAMP_A5` (Fig. 1d):

- Grounded-gate PMOS sense FET M_{sns} ($0.42/8\,\mu$m) stays cut off for $v_{\mathrm{ctrl}} < 1.15$ V, while series NMOS loads $M_{\mathrm{ld1,2}}$ ($2 \times 0.42/8\,\mu$m, biased by v_{bn}, keeping all $L \le 8\,\mu$m) hold `clmp` at 0.2 mV.
- Pull-down NMOS M_{pd} ($6/0.5\,\mu\mathrm{m} = 2 \times 3/0.5\,\mu$m) stays off ($I_D < 0.5$ pA, total leakage 14.3–48.9 nA @ 1.15 V, 61×–215× below the 1-FET diode), yielding 0.00 dB noise and HD3 penalty.
- Above 1.23–1.32 V, the high-gain two-stage loop ($M_{\mathrm{sns}} \rightarrow M_{\mathrm{pd}}$) engages as a brick wall within < 40 mV, capping $f_{\mathrm{VCO}} \le 6.66$ MHz across all 9 extreme corners.
- Miller cap M_c ($4/3\,\mu$m NMOS) stabilizes the clamp loop, cutting overload ringing from 1081 mV to 0.00–0.32 mV while maintaining integrator Tian PM = 72.2° [67.7°–79.8°] and GM = 6.5 dB.

D. Full-Transistor Digital Output Isolation

In `Base_S13`, first-rank `dfxtp_4` cells drove external 1–5 pF mux/pad capacitance directly in parallel with internal `dfxtp_1+xor2_1`, skewing `Q1` vs. `Q2` during back-to-back toggles (causing full-rail XOR glitches stealing up to 14.8 ns of DAC charge) and creating 6.0 ns rise/fall asymmetry. In `V2_A5` (Fig. 1b), `dfxtp_1` drives only internal `dfxtp_1+xor2_1` plus an abutted `buf_4` pin buffer, making DAC pulse integrity invariant over $C_{\mathrm{load}} \in [0.05, 5.0]$ pF.

III. Hand Analysis, Operating Point & Budgets

A. Loop Transfer, Full Scale, and Noise Equations

Cascading the OTA-C integrator and 7-stage VCO phase quantizer yields integrator unity-gain frequency

$$f_{\mathrm{int}} = \frac{1}{2\pi R_{\mathrm{in}} C_{\mathrm{int}}} = \frac{1}{2\pi(49.72\,\mathrm{k\Omega})(2.432\,\mathrm{pF})} = 1.316\,\mathrm{MHz}, \tag{1}$$

and VCO sensitivity $2MK_{\mathrm{VCO}}/f_s = 14(8.48\,\mathrm{MHz/V})/10\,\mathrm{MHz} = 11.87$ LSB/V at TT ($V_{\mathrm{ctrl,lock}} = 0.855$ V). Balancing peak input current against 7 DAC resistors at $V_{DD}/2 = 0.90$ V fixes single-ended full scale:

$$V_{\mathrm{FS,side}} = \frac{7R_{\mathrm{in}}}{R_d}\,\frac{V_{DD}}{2} = \frac{7 \times 49.72\,\mathrm{k\Omega}}{1.0385\,\mathrm{M\Omega}}(0.90\,\mathrm{V}) = 0.302\,\mathrm{V}, \tag{2}$$

or ±0.604 V differential. Nominal dynamic tests use ±0.15 V/side (0.30 V_{pk} diff., −6.0 dBFS) to avoid quantizer clipping across PVT. Referred to the differential input, the front-end noise PSD is

$$S_{v,\mathrm{in}}(f) = 2\left[4kTR_{\mathrm{in}}\left(1 + \frac{R_{\mathrm{in}}}{R_{d,\mathrm{eq}}}\right) + \left(1 + \frac{R_{\mathrm{in}}}{R_{d,\mathrm{eq}}}\right)^2 S_{v,\mathrm{OTA}}(f)\right], \tag{3}$$

where $R_{d,\mathrm{eq}} = R_d/7 = 148.4\,\mathrm{k\Omega}$ and OTA noise gain is 1.335. Shared V_{ref} divider noise is strictly common-mode and cancels in $y = y_N - y_P$.

B. Exact Operating Point, Power, and Noise Breakdown

Table II lists exact BSIM4 TT operating points from `ngspice-47`. Input pair $XM_{1,2}$ operates in moderate-to-weak inversion ($g_m/I_D = 19.0\ \mathrm{V}^{-1}$, $g_m = 219.2\,\mu$S) to maximize transconductance efficiency while preserving $V_{DS} > 3.8\,V_{DS,\mathrm{sat}}$; load $XM_{3,4}$ runs at $g_m/I_D = 9.1\ \mathrm{V}^{-1}$ so $(g_{m3}/g_{m1})^2 = 0.23$ attenuates load noise. Analytical gain $A_0 = g_{m2}(r_{o2} \parallel r_{o4}) = 248$ V/V (47.9 dB) matches AC simulation (47.82 dB) within 0.1 dB. In normal operation, `CLAMP_A5` draws < 0.3 nA ($M_{\mathrm{pd}} < 0.5$ pA), whereas at 1.28 V M_{pd} transconductance surges to 1.01 mS (> 200 μA sink), enforcing a brick-wall ceiling.

Table III summarizes the TT power budget measured across isolated supply rails in full-transistor transient simulation. Total ADC core power is 96.4 μA (173.4 μW at 1.80 V), with `CLAMP_A5` contributing 0.00% (5.5 pA). Driving 16×1 pF external pin loads via `buf_4` adds 69.6 μA (125.4 μW), giving 166.0 μA (298.8 μW) total tile power. Table IV details the BSIM4 integrated differential noise (100 Hz–50 kHz, TT): upsizing $XM_{1,2}$ and $XM_{3,4}$ cuts $M_{1,2}$ flicker noise from 71.3 to 18.8 $\mu\mathrm{V}_{\mathrm{rms}}$ (14.4× variance reduction), raises resistor thermal noise share from 0.9% to 9.2%, and confirms 0.00% noise from `CLAMP_A5`.

IV. Simulation Results

All simulations ran in `ngspice-47` with the tapeout-locked SkyWater `sky130A` BSIM4v5 PDK (`open_pdks 0536d02d`). AC stability and `.noise` runs disable `option klu` (avoiding KLU AC/noise inaccuracies in `ngspice-47`), while transient tone signoff enforces $\Delta t_{\max} = 0.5$ ns, reltol = 10^{-4}, and Gear integration so digital edge placement never injects artificial DAC jitter (~ 25 dB error at 2 ns step). Every transient includes 500 Ω series resistance on `ua[0:1]` modeling Tiny Tapeout's analog mux.

A. Integrator Stability and BSIM4 Noise Performance

Fig. 2(a) shows exact Tian closed-loop integrator return ratio $T(f)$ [4] across extreme PVT corners with VCO input loading, 30 fF node parasitics, and $R_{\mathrm{in}} \parallel R_{d,\mathrm{eq}}$. At TT, `V2_A5` achieves PM = 72.2° at $f_{ug} = 4.95$ MHz and GM = 6.5 dB; across `ss_hh`/85°C/1.62 V and `ff_ll`/−20°C/1.98 V, PM ∈ [67.7°, 79.8°] and GM ∈ [6.5, 7.2] dB. Fig. 2(b) plots differential BSIM4 input-referred noise PSD from 10 Hz to 500 kHz: `V2_A5` cuts integrated noise from 74.6 to 22.9 $\mu\mathrm{V}_{\mathrm{rms}}$ (+10.2 dB), reaching 79.3 dB (81.1 dB in 20 kHz) at TT and 78.3 dB at worst-case `ss_hh`/85°C/1.62 V, with 0.00 dB difference vs. `V2_NoClmp`.

B. Brick-Wall Anti-Latchup and Digital Isolation Proof

Fig. 3(a) shows VCO tuning $f_{\mathrm{VCO}}(V_{\mathrm{ctrl}})$ with `CLAMP_A5`'s ceilings and I_{clamp} inset. While an unclamped OTA drives f_{VCO} to 8.99–9.33 MHz inside the > 7.5 MHz latch-up zone at `ss_ll`/85°C/1.98 V and `fs_ll`/1.98 V, `CLAMP_A5` engages as a vertical wall above 1.23 V while leaking only 14.3–48.9 nA at 1.15 V (61×–215× below the 1-FET diode's 1.1–4.5 μA). Under forced $v_{\mathrm{ctrl}} = V_{DD}$ no-reset startup or 15 μs rail overdrive at `fs_ll`/1.98 V (Fig. 3(b)), `Base_S13` latches permanently at 8.49 MHz, whereas `V2_A5` clamps cleanly ($f_{\max} \le 6.66$ MHz across all 9 corners, ringing ≤ 0.32 mV) and recovers to 2.50 MHz lock in < 3 μs across 10/10 schematic stress tests.

Fig. 3(c) shows the full-transistor (`dig=0`, BSIM4 `sky130_fd_sc_hd`) isolation sweep over $C_{\mathrm{load}} = 0.05$–5.0 pF. With baseline `dfxtp_4`, back-to-back XOR glitches collapse to 0 V (inset at 3 pF), stealing 1.92–7.80 ns (TT) and 3.73–14.82 ns

TABLE II
EXACT BSIM4 TRANSISTOR OPERATING POINTS AT TYPICAL CORNER (tt, 27°C, V_{DD} = 1.80 V)

Block	Device (Type)	W/L (μm)	$\lvert I_D\rvert$ (μA)	$\lvert V_{GS}\rvert$ (V)	$\lvert V_{DS}\rvert$ (V)	g_m (μS)	g_m/I_D (V^{-1})	r_o (kΩ)	Region
so_bias	XM_b (NMOS, 4 × 2/2)	8/2	24.42	0.767	0.767	219.7	9.0	737	Sat. (diode)
ota5t	$XM_{1,2}$ (NMOS, 4 × 12/3)	48/3	11.52	0.652	0.325–0.656	219.2	19.0	1031–1386	Weak/Mod. Sat.
	$XM_{3,4}$ (PMOS, 4 × 4/2)	16/2	11.52	1.228	0.896–1.228	105.2	9.1	6222–8275	Strong Sat.
	XM_5 (NMOS, 4 × 2/2)	8/2	23.04	0.767	0.248	202.4	8.8	98.3	Sat. (V_{dsat} 0.20 V)
CLAMP_A5	M_{sns} (PMOS) norm / clmp†	0.42/8	0.0003 / 0.132	0.904 / 1.280	0.903 / 0.292	0.005 / 0.89	— / 6.7	> 10^8 / 26.5M	Cutoff / Sat.
	$M_{ld1,2}$ (2×NMOS) norm / clmp	0.42/8	0.0003 / 0.132	0.767 / 0.705	0.0001 / 0.925	0.001 / 1.53	— / 11.6	401 / 281M	Triode / Sat.
	M_{pd} (NMOS, 2 × 3/0.5) norm / clmp	6/0.5	< 10^{-6} / 208‡	0.0002 / 0.988	0.904 / 1.280	10^{-5} / 1013	— / 4.9	> 10^9 / 81.8	Off / Strong Sat.
	M_c (NMOS Miller cap)	4/3	0	0.903 / 0.292	0	0	—	C_{gg} = 88.6 fF	MOS Cap
vco_core	XM_1 (V-to-I NMOS @ 0.905 V)	4/1	1.12	0.648	0.434	23.8	21.2	5252	Weak/Mod. Sat.
	XM_{pd}, XM_{p2} (PMOS mirror)	1/1	1.12	1.109	1.08–1.11	11.3	10.0	50.8M	Sat.
	XM_{nd} (NMOS mirror)	0.5/1	1.12	0.721	0.721	13.9	12.4	8183	Sat.

Passives (TT): R_{in} = 49.72 kΩ (L = 8.6), R_d = 1.039 MΩ (L = 181.8), R_b = 42.30 kΩ (L = 7.3), $R_{t,bt}$ = 200.4 kΩ (L = 35), R_{vco} = 229.7 kΩ, C_{int} = 2.432 pF.
†"norm" at v_{ctrl} = 0.904 V; "clmp" at TT ceiling 1.28 V. ‡Sinking capacity > 200 μA vastly exceeds 23 μA OTA pull-up, locking brick-wall ceiling at 1.27 V.

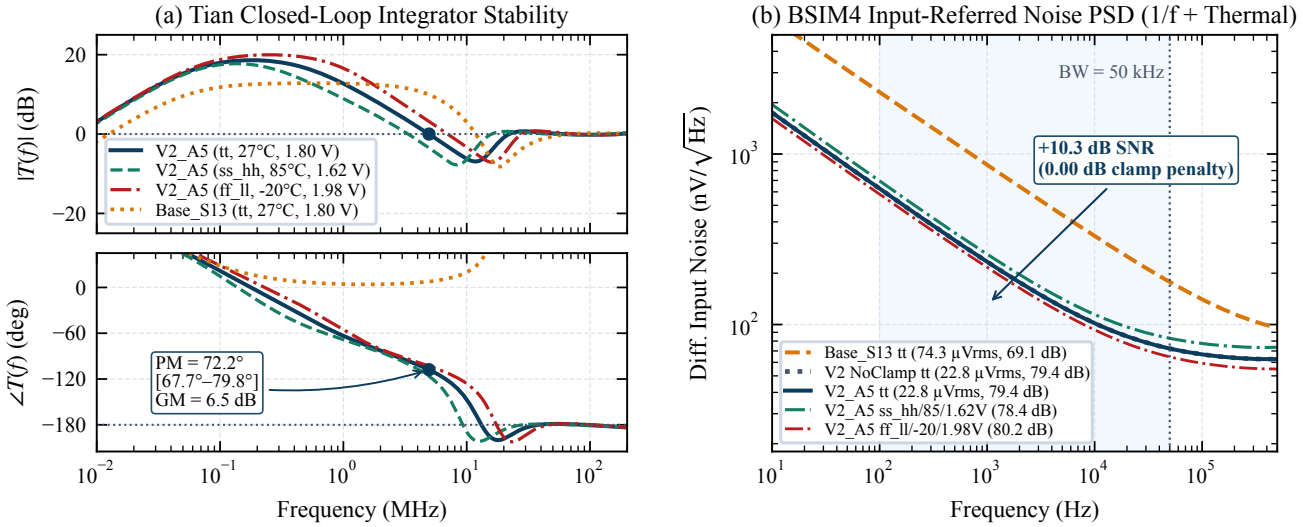


Fig. 2. (a) Exact Tian closed-loop integrator stability $|T(f)|$ and $\angle T(f)$ across extreme PVT corners (tt/27°C/1.80 V, ss_hh/85°C/1.62 V, ff_ll/−20°C/1.98 V) vs. Base_S13, confirming PM = 72.2° [67.7°–79.8°] and GM = 6.5 dB [6.5–7.2 dB]; (b) BSIM4 differential input-referred noise PSD (10 Hz–500 kHz), demonstrating +10.2 dB noise-floor reduction (74.6 → 22.9 μV_{rms}), worst-case ss_hh/85°C/1.62 V ceiling of 78.3 dB, and 0.00 dB penalty from CLAMP_A5.

TABLE III
TT POWER BREAKDOWN (1.80 V, 27°C, MID-SCALE LOCK)

Sub-Block	I_{DD} (μA)	Power (μW)	Share
Shared OTA Bias (R_b, X_{Mb})	24.42	43.95	14.7%
Shared V_{ref} Divider (R_t, R_{bt})	4.49	8.08	2.7%
2× 5T OTA ($XM_{1...5}$)	46.09	82.96	27.8%
2× Active Clamp (CLAMP_A5, norm.)	5.5 × 10^{-6}	≈ 0.00	**0.0**%
2× VCO V-to-I & Mirror	3.87	6.97	2.3%
2× 7-Stage Current-Starved Ring	2.55	4.60	1.5%
2× Int. Dig. (dfxtp_1, xor2_1) + RDAC	14.93	26.88	9.0%
ADC Core Subtotal (No Ext. Loads)	**96.36**	**173.44**	**58.0**%
2× Ext. Buffers (16 × buf_4 @ 1 pF)	69.64	125.36	42.0%
Total Tile (Incl. 16 × 1 pF Loads)	**166.00**	**298.80**	**100.0**%

TABLE IV
BSIM4 DIFF. INPUT-REFERRED NOISE BREAKDOWN (100 Hz–50 kHz, TT)

Noise Source	Base_S13		V2_A5 (Final)	
	Var.	RMS (μV)	Var.	RMS (μV)
$XM_{1,2}$ Flicker (1/f)	90.50%	71.34	65.94%	18.78
$XM_{1,2}$ Thermal	0.83%	6.84	4.31%	4.80
$XM_{3,4}$ Flicker (1/f)	7.49%	20.52	19.43%	10.19
$XM_{3,4}$ Thermal	0.26%	3.83	1.05%	2.37
XM_5, X_{Mb} (Tail Bias)	< 0.01%	0.39	0.01%	0.27
CLAMP_A5 (All 5 FETs)	—	—	**0.00**%	**0.00**
R_{in} (49.7 kΩ) Thermal	0.69%	6.22	6.92%	6.08
7 × R_d (1.04 MΩ) Thermal	0.23%	3.60	2.32%	3.52
Total (100 Hz–50 kHz)	**100**%	**74.6**★	**100**%	**22.9**★
SNR (@ 0.15 V/s) / **FS DR**	69.1 / 75.1 dB		**79.3** / **85.3** dB (+**10.2**)	

★Exact inoise_spectrum integral (20 kHz SNR = 81.1 dB).

(ss_hh/85°C/1.62 V), while rise/fall asymmetry reaches 0.58–6.01 ns. With dfxtp_1+buf_4, internal glitch charge theft stays load-invariant at 0.103 ns (TT) / 0.165 ns (ss_hh, V_{min} = 1.59 V, 19×–90× lower) and asymmetry drops to 0.028–0.030 ns (20×–215× lower across 1–5 pF).

C. True In-Band 14.65 kHz Dynamic Linearity

Unlike earlier 24.4 kHz tests that placed HD3 out-of-band (73 kHz), all sign-off runs apply coherent f_{in} = 14.648 kHz (N = 2048, bin 3, ±0.15 V/side, 3-bin Hann scoring) so both HD2 = 29.30 kHz and HD3 = 43.95 kHz lie inside the 50 kHz band. In Fig. 4(a), V2_A5 follows +40 dB/dec second-order shaping and achieves 71.8 dB SNDR (HD2 = −75.9, HD3 = −76.1 dBc) at TT schematic, 71.5 dB (HD3 = −75.0 dBc) at sf, 68.9 dB (HD3 = −70.3 dBc) at ff_hh/−20°C (+24 dB better HD3 than the 1-FET diode's −46 dBc), and 70.1 dB (HD3 = −71.9 dBc) in full-transistor flat-PEX TT.

V. PVT, MISMATCH, AND PHYSICAL SIGN-OFF

A. 21-Corner PVT + R/C + V_{DD} and 16-Seed Mismatch MC

Table V and Fig. 4(b) report the 21-corner PVT matrix across MOSFET skews (tt, ss, ff, sf, fs), SKY130 passive R/C corners (hh, hl, lh, ll), temperature (−20 to 85°C), and supply (1.62, 1.80, 1.98 V), plus 16-seed tt_mm mismatch MC at 14.65 kHz. Every

TABLE V
21-CORNER PVT+R/C+V_{DD} ± 10% & 16-SEED tt_mm MC (14.65 kHz, 50 kHz BW)

Corner (T, V_{DD})	SNDR	SNR	HD2	HD3
tt (27°C, 1.80/1.98 V)	71.6/73.2	77.7/78.8	−77.6/−76.0	−74.6/−80.6
tt (27°C, 1.62 V)	71.2	78.2	−76.9	−73.9
lh/ll/hh/hl (27°C, 1.8 V)	70.2–73.4	78.5–80.4	−76.2–−76.5	−72.3–−80.1
ss_hh (85°C, 1.80/1.62 V)	68.5/68.7	73.4/78.5	−76.3/−75.3	−71.5/−70.4
ss_ll (85°C, 1.80/1.98 V)	73.0/73.3	77.9/78.1	−76.3/−77.6	−79.8/−78.5
ff_hh (−20°C, 1.80/1.62 V)	70.5/66.9	80.0/78.7	−76.7/−76.6	−72.4/−67.7
ff_ll (−20°C, 1.80/1.98 V)	70.4/71.1	78.1/78.4	−76.0/−76.1	−73.1/−74.2
fs_hh/ll (27°C, 1.80 V)	69.2/71.2	78.9/77.9	−77.6/−78.0	−70.5/−73.5
fs_ll (27°C, 1.98 V)	71.0	79.6	−76.2	−73.5
sf_hh/ll (27°C, 1.80 V)	71.3/72.6	78.3/80.3	−77.1/−76.2	−74.1/−76.5
sf_hh (27°C, 1.62 V, min)	63.4	78.1	−76.6	−63.7
17 (1.8/1.98 V) Range	**68.5–73.4**	**73.4–80.4**	−76.0–−78.0	−70.5–−80.6
16 MC (Min/Med/Max)	**68.1/71.1/71.7**	**71.4–80.8**	≤ −72.6	≤ −72.5

Units: SNDR/SNR in dB; HD2/HD3 in dBc. MC (N = 16): σ_{SNDR} = 1.17 dB, σ_{dc} = 0.016 LSB.

corner locks cleanly to $f_s/4$. All 17 nominal/high-V_{DD} corners (1.80/1.98 V) achieve 68.5–73.4 dB SNDR (median 71.2 dB) with HD3 = −70.5 to −80.6 dBc. At 1.62 V (−10%), TT stays at 71.2 dB and ss_hh/85°C at 68.7 dB, dipping to 63.4 dB only at extreme sf_hh/1.62 V due to headroom compression on XM_1 (HD3 = −63.7 dBc). Across 16 tt_mm MC seeds, SNDR spans 68.1–71.7 dB (median 71.1 dB, σ = 1.17 dB), worst HD2/HD3 remain below −72.6/−72.5 dBc, and differential DC offset has σ = 0.016 LSB.

B. Physical Layout and Sign-Off Verification

Fig. 5 presents the procedurally generated layout (layout/gen_layout.py, 161.0 × 225.76 μm^2). Vertical mirror symmetry isolates P and N halves while centering the shared $D\,N_1\,P_1\,P_2\,N_2\,D$ VCO bias resistor array. Each RDAC uses 42 matched poly strips plus dummies; each OTA uses interdigitated A A B B B B A A common-centroid fingers above its 2 × (24 × 25 μm^2) MIM capacitors; and 699 × decap_12 cells stiffen VDPWR/VGND.

Table VI records complete V2_03 physical sign-off and flat C-only PEX verification (234 KB, 1,248 BSIM4/PDK devices, 2,443 caps, 0 neg. caps/as/ps). Eight conb_1 tie-high cells for uio_oe[7:0] clear the Netgen 1.5.324 port-merger warning, yielding Circuits match uniquely. (195 dev, 144 net, 54/54 pins), 0 DRC, and 16/16 TT precheck (0 met5 OBS, 0 output antenna). All 4/4 flat-PEX unreset/overload runs lock at 2.50–2.53 MHz, and all 6/6 flat-PEX 14.65 kHz corners sustain 69.0–70.6 dB SNDR (77.7–81.9 dB SNR, HD2 = −76.8 to −77.8 dBc, HD3 = −70.4 to −72.5 dBc, f_P/f_N = 2.49–2.50 MHz, uio_oe = 1.80 V), lifting sf flat-PEX HD3 by +11.5 dB over Base_S13 (−59.0 → −70.5 dBc) even in-band.

TABLE VI
PHYSICAL SIGN-OFF (V2_03) & FULL-TRANSISTOR FLAT-PEX VERIFICATION

A. Physical Rule & Extraction Sign-Off	
Magic DRC (Precheck GDS)	**0 errors**
Netgen 1.5.324 LVS	**Unique** (195 dev, 144 net, 54/54 pin)
Tiny Tapeout Precheck	**16/16 PASS** (0 met5 OBS, 0 out ant.)
Flat C-Only PEX Netlist	234 KB, 2,443 caps, 0 neg. caps/as/ps

B. Full-Transistor Flat-PEX Anti-Latchup Stress (4/4 PASS)		
PEX Stress Case	**Locked f_P/f_N (MHz)**	**Status**
pex_tt_norst (no rst_n, 1.80 V)	2.52 / 2.52	**PASS**
pex_fsll198_norst (no rst_n, 1.98 V)	2.52 / 2.51	**PASS**
pex_fsll198_ovl (rail OVL, 1.98 V)	2.52 / 2.50	**PASS**
pex_ssll85_198ovl (OVL, 85°C, 1.98 V)	2.52 / 2.53	**PASS**

C. Full-Transistor Flat-PEX 14.65 kHz Tone (6/6 PASS, 16 × 1 pF)		
Corner (T, V_{DD})	**SNDR / HD2 / HD3**	**I_{DD} (μA)**
tt (27°C, 1.80 V)	70.1 / −77.8 / −71.9	173.5
ss (85°C, 1.80 V)	69.0 / −77.4 / −70.4	176.1
ff (−20°C, 1.80 V)	69.3 / −76.8 / −70.7	173.2
sf (27°C, 1.80 V)	69.3 / −76.8 / −70.5	177.1
fs (27°C, 1.80 V)	70.6 / −76.9 / −72.5	170.9
fs_ll (27°C, 1.80 V)	70.4 / −76.9 / −72.5	175.4

VI. DISCUSSION AND ARCHITECTURAL TRADE-OFFS

Several alternatives were quantitatively evaluated and rejected during closure:

1. **1-FET Diode vs. Two-Stage Active Clamp:** A single grounded-gate PMOS diode (8/0.5 μm) leaked 3.1 μA at 1.15 V, degrading ff_hh/−20°C HD3 to −46 dBc. The Miller-compensated two-stage CLAMP_A5 sharpens the turn-on knee by 61×–215× (14–49 nA @ 1.15 V), restoring HD3 = −70.3 dBc (+24 dB). Splitting the load into two series 0.42/8 μm FETs ($M_{\mathrm{ld1,2}}$) rather than one 0.42/20 μm device keeps all FETs within well-calibrated $L \le 8\,\mu$m BSIM4 bins with a compact

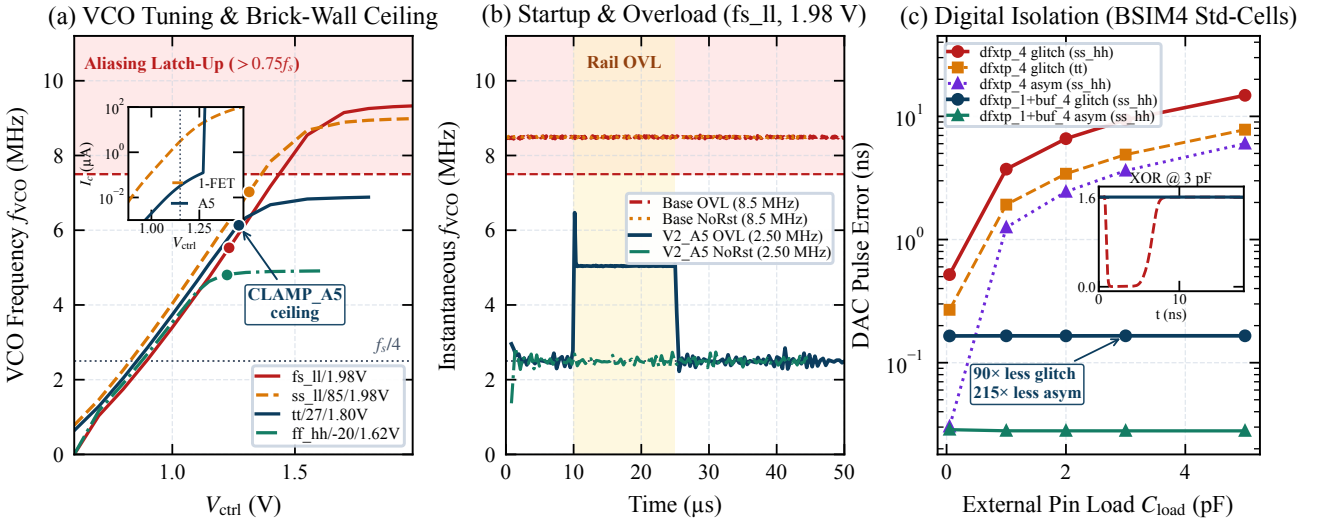


Fig. 3. Verification of anti-latchup clamping and digital output isolation: (a) VCO tuning $f_{VCO}(V_{ctrl})$ showing unclamped runaway (> 9 MHz) into the > 0.75f_s latch-up zone vs. CLAMP_A5 brick-wall ceilings (≤ 6.66 MHz closed-loop; inset compares $I_{clamp}(V_{ctrl})$ vs. the leaky 1-FET diode, cutting 1.15 V leakage 61×–215× to 14.3–48.9 nA); (b) forced $v_{ctrl} = V_{DD}$ no-reset startup and 10–25 μs rail overload at worst corner fs_ll/1.98 V, where Base_S13 latches at 8.49 MHz while V2_A5 locks at 2.50 MHz; (c) full-transistor (dig=0) BSIM4 std-cell isolation sweep over C_{load} = 0.05–5.0 pF, reducing XOR glitch charge theft 19×–90× and rise/fall asymmetry 20×–215× across 1–5 pF (inset: XOR bp glitch at 3 pF, ss_hh).

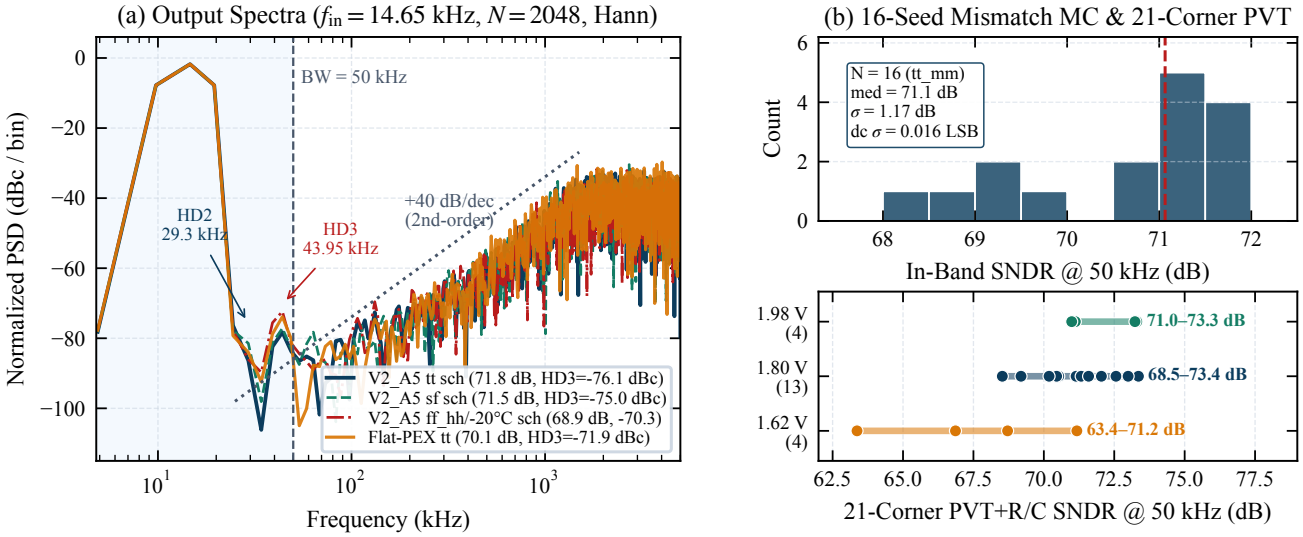


Fig. 4. (a) True in-band 14.65 kHz (N = 2048, bin 3, Hann, Δt_{max} = 0.5 ns, reltol = 10^{-4}) differential output spectra for `V2_A5` schematic (`tt`, `sf`, `ff_hh`/−20°C) overlaid with full-transistor flat-PEX `tt` (70.1 dB SNDR, HD3 = −71.9 dBc, 16 × 1 pF loads), showing HD2 = 29.3 kHz and HD3 = 43.95 kHz strictly in-band with +40 dB/dec shaping; (b) top: 16-seed `tt_mm` mismatch MC SNDR histogram (68.1–71.7 dB, med. 71.1 dB, σ = 1.17 dB, diff. DC σ = 0.016 LSB); bottom: 21-corner PVT + R/C + V_{DD} ± 10% SNDR distribution by supply.

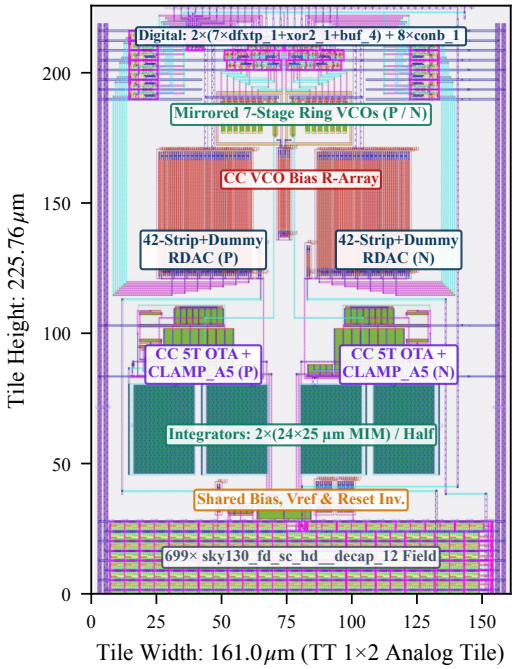


Fig. 5. Annotated layout of `tt_um_arcadia1_vco_adc` (161.0 × 225.76 μm^2, `sky130A` 1 × 2 tile) highlighting mirrored digital banks, 7-stage VCOs, CC bias resistor array, RDACs, CC OTAs with `CLAMP_A5`, MIM caps, and 699×`decap_12`.

layout footprint.

2. **Half-Cycle DAC Resampling:** Inserting a half-cycle resampling latch before the RDAC was investigated during early S13 debugging, but step-size ablations proved the observed noise degradation came from a 2 ns transient step artifact. Since extra loop delay erodes stability margin without improving real quantization noise, resampling was removed.

3. **Low-V_{DD} Headroom Bound:** At −10% supply (1.62 V) with slow-NMOS/fast-PMOS and high-R (`sf_hh`), losing 180 mV of swing headroom pulls HD3 to −63.7 dBc (63.4 dB SNDR) at ±0.15 V/side while remaining completely latch-up-free; backing off amplitude by 2 dB or holding $V_{DD} \geq 1.75$ V restores > 70 dB SNDR across all corners.

4. **Silicon Characterization Plan:** On fabricated SKY26e silicon, an RP2350 PIO+DMA test script (`test/capture_vco_adc.py`) will supply the 10 MHz clock and stream all 16 outputs (`uo_out[7:0]`, `uio[7:0]`) continuously after a 30 μs post-reset settling interval. Checking `MONP`/`MONN` at 2.50 MHz confirms mid-scale lock before running `test/decode_vco_adc.py` for differential FFT/SNDR evaluation.

VII. Conclusion

A 1.8-V pseudo-differential second-order closed-loop VCO ΔΣ ADC (`tt_um_arcadia1_vco_adc`) has been designed, verified, and signed off in `sky130A` inside a 161.0×225.76 μm^2 Tiny Tapeout 1 × 2 tile. Three targeted upgrades—a +10.2 dB lower-noise CC 5T OTA (22.9 μV_{rms}, 79.3 dB ceiling, PM = 72.2°), a zero-static-power 5-FET Miller active clamp eliminating > 7.5 MHz latch-up (0.00 dB noise/HD3 penalty), and `dfxtp_1+buf_4` pin isolation cutting BSIM4 DAC glitch/asymmetry 19×–215×—yield 71.8 dB TT schematic SNDR at 14.65 kHz (68.5–73.4 dB across 17 1.80/1.98 V PVT+R/C corners, 71.1 dB MC median) and 69.0–70.6 dB SNDR (77.7–81.9 dB SNR, HD3 = −70.4 to −72.5 dBc) across all 6 full-transistor flat-PEX corners at 173.4 μW core power (312 μW PEX w/ 16 × 1 pF), with 0 DRC, unique LVS (54/54 pins), 16/16 precheck, and 4/4 flat-PEX latch-up passes.

References

[1] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time ΣΔ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[2] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec. 2010.

[3] X. Xing and G. G. E. Gielen, "A 42-fJ/step-FoM two-step VCO-based delta-sigma ADC in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 714–723, Mar. 2015.

[4] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert, "Striving for small-signal stability," *IEEE Circuits Devices Mag.*, vol. 17, no. 1, pp. 31–41, Jan. 2001.

[5] SkyWater Technology Foundry, "SKY130 Open-Source Process Design Kit (`sky130A`, `open_pdks 0536d02d`)," Tiny Tapeout SKY26e Analog Shuttle Documentation, 2026.